SL.NO:2285 **SUBJECT CODE:43321C01**

VINAYAKA MISSIONS RESEARCH FOUNDATION
(Deemed to be University)
M.E./ M.TECH DEGREE EXAMINATIONS- APRIL -2022
VLSI DESIGN
FIRST SEMESTER
ELECTRONIC DESIGN AUTOMATION TOOLS

(Candidates admitted under 2021 Regulations-SCBCS)

Time : Three Hours Maximum Marks:100 Marks

Answer **ALL** questions

Part-A (10 x 2 =20 Marks)

1 Define Paging.
2 Define time constant of RC circuit.
3 Tell what is meant by continuous assignment statement in verilog HDL.
4 Recite Switch-level modeling.
5 Contrast scalars and vectors.
6 State the use of packages.
7 Recall the static variable.
8 Recite RAM processor.
9 Identify how to run a program from within Vi.
10 Recite the advantages and applications of sample and hold circuits.

Answer **Any FIVE** questions

Part-B (5 x10 =50 Marks)

11 a. Discuss how computer aided design differs from conventional design

OR

b. Explain the synthesis procedure in Verilog HDL.

12 a. Explain UNIX OS and mention the properties.

OR

b. Explain two application areas of computer aided design.

13 a. Describe the expression for the Fermi level energy in n – type semiconductor.

OR

b. Explain the drift and diffusion currents for PN diode.

14 a. Explain the concept of gate delay in VERILOG with example.

OR

b. Discuss value change dump file.

15 a. Discuss level of design description.

(P.T.O)

OR

b. Discuss in detail about implementing always block logic in program block.

16 a. Illustrate how SV is more random stable than Verilog.

OR

b. Discuss whether randomization is successful or not.

17 a. Explain the basic processors and hardware units in the embedded system.

OR

b. Explain in detail about interrupt latency and their solutions

18 a. Explain the concept of Timing control in VERILOG.

OR

b. Tabulate the differences between data types logic, reg and wire.

Answer ALL questions

PART-C (2 x 15 = 30)

19 a. Examine PCB design flow chart.

OR

b. Describe the Emerging Applications in Embedded systems.

20 a. Explain A/D and D/A with neat circuit diagram.

OR

b. Narrate how embedded system is used in smart card technology.

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SL.NO:2285

SL.NO:2277 **SUBJECT CODE:43321C02**

VINAYAKA MISSIONS RESEARCH FOUNDATION
(Deemed to be University)
M.E./ M.TECH DEGREE EXAMINATIONS- APRIL -2022
VLSI DESIGN
FIRST SEMESTER
RTL SIMULATION AND SYNTHESIS WITH PLDS

(Candidates admitted under 2021 Regulations-SCBCS)

Time : Three Hours Maximum Marks:100 Marks

Answer **ALL** questions

Part-A (10 x 2 =20 Marks)

1 Define reset recovery time
2 Recite structural gate-level modelling.
3 Recite Verilog-AMS.
4 Define ESD protection.
5 Define reliability.
6 Label the state diagram of Moore state machine
7 Identify the importance of registered output.
8 Identify the parameters that differentiate chip design and block level design.
9 Define Maze routing.
10 Recite the protocol used for connection establishment.

Answer **Any FIVE** questions

Part-B (5 x10 =50 Marks)

11 a. Examine the Synthesis of finite state machines.

OR

b. Explain the derivations of state machine changes.

12 a. Explain about Clock Skew and Clock Jitter.

OR

b. Examine the signal assignments in the VHDL.

13 a. Explain conditional operator and operator precedence in VERILOG.

OR

b. Contrast ROM, PAL, PLA and PLD.

14 a. Interpret the differences between FPGA’s and CPLD’s.

OR

b. Explain the routing architecture of field programmable gate arrays.

15 a. Explain the advantages of Scaling in Low power VLSI Design.

(P.T.O)

OR

b. Examine any two BIST concepts.

16 a. Examine how testing is made easier using circuit design.

OR

b. Explain Soft IP.

17 a. Examine VHDL operators and explain function of each one with examples.

OR

b. Examine the prototyping power saving features.

18 a. Examine hard IP cores with advantages.

OR

b. Discuss on the use of external hard IP during prototype.

Answer ALL questions

PART-C (2 x 15 = 30)

19 a. a) Explain the need and design strategies for multi-clock domain design.
b) Explain about the term ‘synchronization’. Give its significance.

OR

b. Explain the structural design methodology with the Verilog HDL.

20 a. Analyze the Masked Gate Array ASIC.

OR

b. Examine following concepts with examples:
   a. Verilog Strings
   b. Verilog Constants
   c. Verilog Operations.
   d. Verilog Variables.

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SL.NO:2264 **SUBJECT CODE:43321C03**

VINAYAKA MISSIONS RESEARCH FOUNDATION
(Deemed to be University)
M.E./ M.TECH DEGREE EXAMINATIONS- APRIL -2022
VLSI DESIGN
FRIST SEMESTER
DESIGN OF ASICS

(candidates admitted under 2021 Regulations)

Time : Three Hours Maximum Marks:100 Marks

Answer **ALL** questions

Part-A (10 x 2 =20 Marks)

1 Define Programmable Interconnects
2 State the importance of layout in ASIC design.
3 Define a launch edge.
4 List out the goals of detailed routing.
5 State the difference between ASIC design and SoC design.
6 Differentiate between the standard cell-based ASICs and full custom ASIC.
7 Identify how granularity of logic block influences the performance of an FPGA.
8 Identify the objectives of placement algorithm.
9 Define Circuit extraction.
10 Recite applications of SoC.

Answer **Any FIVE** questions

Part-B (5 x10 =50 Marks)

11 a. Explain the performance & characteristics for the Cell based ASIC design styles.

OR

b. Contrast in detail about PLA and PAL devices.

12 a. Describe the techniques for initial placement.

OR

b. Discuss on how signal integrity is related to timing.

13 a. Contrast between DRC and LVS.

OR

b. Sketch the design of standard cell three input NAND gate and respective layout diagram.

14 a. Discuss Partitioning in system design.

OR

b. Examine the different levels at which partitioning is carried out.

15 a. Explain logic synthesis.

(P.T.O)

OR

b. Explain Max Timing Equation.

16 a. Explain GDS in detail.

OR

b. Examine refining of timing analysis. Explain breaking timing arcs in cells.

17 a. Contrast between LEV and LVS

OR

b. Explain Platform-Based SoC design

18 a. Discuss NoC for SoC Design

OR

b. Discuss on the need to consider the I/O and power constraints early in the floorplanning process.

Answer ALL questions

PART-C (2 x 15 = 30)

19 a. Explain floorplanning of a cell-based ASIC.

OR

b. Discuss the Common LVS issues and their debug.

20 a. Explain Simulated annealing algorithm for placement.

OR

b. Explain some of methodologies used in DFM.

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SL.NO:2263 **SUBJECT CODE:43321P01**

VINAYAKA MISSIONS RESEARCH FOUNDATION
(Deemed to be University)
M.E./ M.TECH DEGREE EXAMINATIONS- APRIL -2022
VLSI DESIGN
FIRST SEMESTER
ELECTIVE - MODELLING AND SYNTHESIS WITH VERILOG HDL

(Candidates admitted under 2021 Regulations-SCBCS)

Time : Three Hours Maximum Marks:100 Marks

Answer **ALL** questions

Part-A (10 x 2 =20 Marks)

1 List the various levels of design description in verilog HDL.
2 Define functional Bifurcation.
3 Give the use of multiple always blocks in programming.
4 Name the basic memory components.
5 Recall display Task.
6 Define basic switch primitive.
7 Infer about force – release construct
8 Recite Feedback model.
9 Define specify block.
10 Compare file based tasks and functions.

Answer **Any FIVE** questions

Part-B (5 x10 =50 Marks)

11 a. Write up counter test bench, simulation results.

OR

b. Categorise the advantages of multiple always blocks with example.

12 a. Illustrate Gate level Modeling with Examples.

OR

b. Design up counter coding procedural assignment.

13 a. Discuss Continuous Assignment Structures.

OR

b. Explain combining assignment and net declarations with examples.

14 a. Describe various descriptive styles available for hardware modeling using Verilog HDL.

OR

b. Design Verilog module for CMOS flip-flop.

(P.T.O)

15 a. Write the Verilog code for half sub-tractor using CMOS switches.

OR

b. Write about basic switch primitives.

16 a. Summarize the VLSI design flow with a neat diagram.

OR

b. Write a short note on, (a). Functional bifurcation (b). Intra-assignment delays.

17 a. Develop a VERILOG code for the 4x1 multiplexer using three state logic.

OR

b. Explain the block diagram of phase locked loop for clock generation.

18 a. Explain continuous assignment structures with examples.

OR

b. Design code, test bench, results for CMOS switch with a single control line.

Answer ALL questions

PART-C (2 x 15 = 30)

19 a. Explain stratified event queue.

OR

b. Sketch the block diagram for test bench for post synthesis design verifications.

20 a. Explain the following concepts:
i) Verilog strings
ii) Verilog constants
iii) Verilog operations
iv) Verilog variables

OR

b. Write short notes on gray-code counter. Also design a Verilog module for the same.

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